IN THE CLAIMS:

1-16. (cancelled)

17. (currently amended) A data processor formed on a single chip, comprising:

a central processing unit executing a plurality of instructions;

a clock pulse generator generating a plurality of clock signals; and

a mode register accessed by the central processing unit, ;

wherein the data processor operates in accordance with a plurality of operation modes based on the mode register, wherein the plurality of operation modes comprise operation modes of the data processor, ;

wherein the operation modes include a first operation mode, a second operation mode, and a third operation mode, ;

wherein the central processing unit executes instructions and receives a clock signal from the clock pulse generator in the first operation mode, ;

wherein the central processing unit and the clock pulse generator halt operation in the second operation mode, ; and

wherein the central processing unit halts executing the instructions and the clock pulse generator generates clock signals in the third operation mode.

18. (previously presented) The data processor according to claim 17, wherein the data processor includes a control terminal, and wherein the data processor changes operation from the second operation mode to the first operation mode in response to the control terminal receiving a predetermined level signal.

19. (previously presented) The data processor according to claim 17, wherein the data processor includes an external interrupt receive terminal which receives an interrupt request from outside of the data processor, and wherein the data processor changes operation from the second operation mode to the first operation mode in response to the external interrupt receive terminal receiving a predetermined level signal.

20. (previously presented) The data processor according to claim 17, wherein the data processor includes a reset terminal, and wherein the data processor changes operation from the second operation mode to the first operation mode in response to the reset terminal receiving a predetermined level signal from outside of the data processor.

21. (previously presented) The data processor according to claim 17, wherein the clock pulse generator halts providing a generated clock signal to the central processing unit in the third operation mode.

22. (previously presented) The data processor according to claim 17, wherein the data processor includes a data transfer controller that controls data transfer between the data processor and outside of the data processor, wherein the plurality of operation modes further includes a fourth operation mode, and wherein the clock pulse generator provides a clock signal to the central processing unit and halts providing a generated clock signal to the data transfer controller in the fourth operation mode.